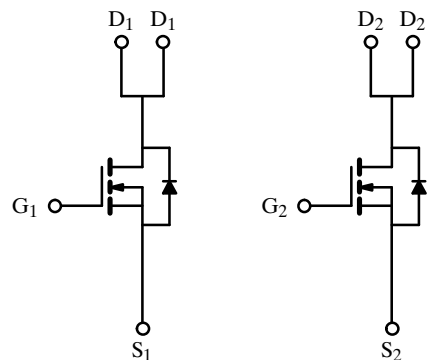
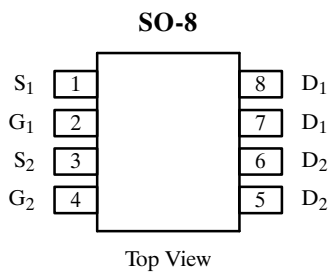


Dual N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.05 @ $V_{GS} = 4.5$ V	± 5.0
	0.06 @ $V_{GS} = 3.0$ V	± 4.2
	0.08 @ $V_{GS} = 2.5$ V	± 3.6



N-Channel MOSFET

N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 5.0
		$T_A = 70^\circ\text{C}$	± 4.0
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 48	A
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2
		$T_A = 70^\circ\text{C}$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1227.

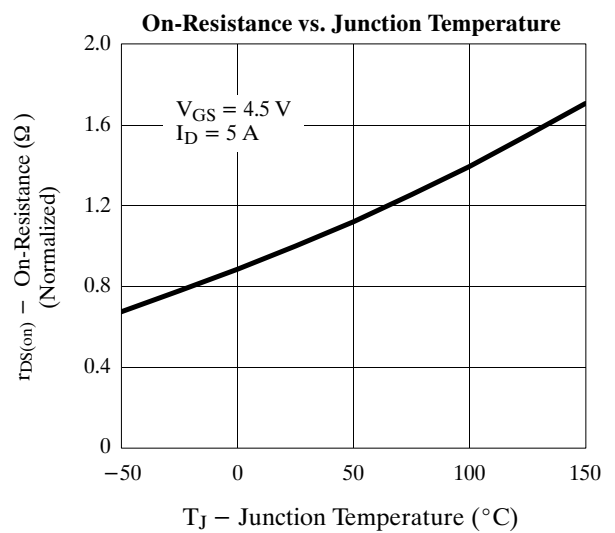
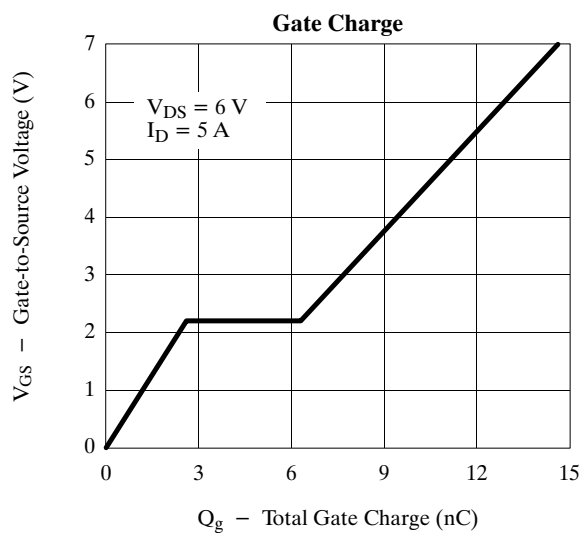
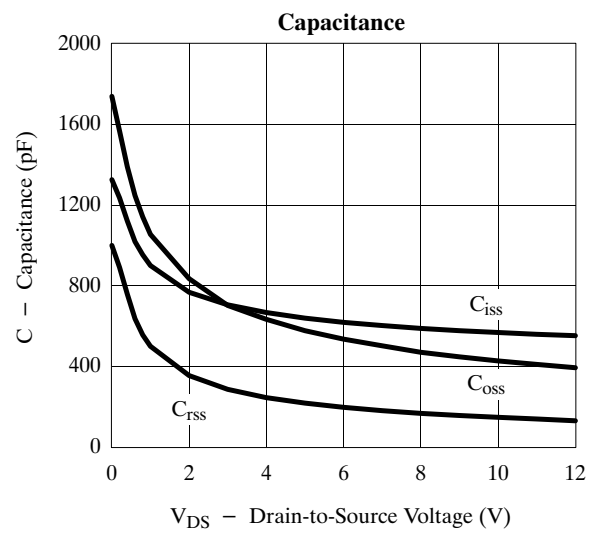
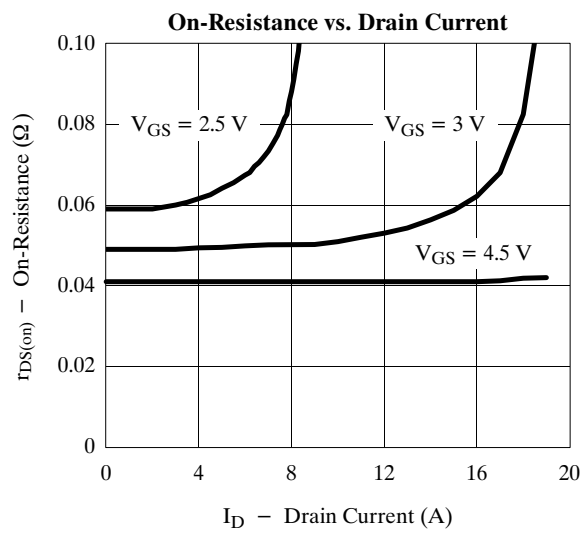
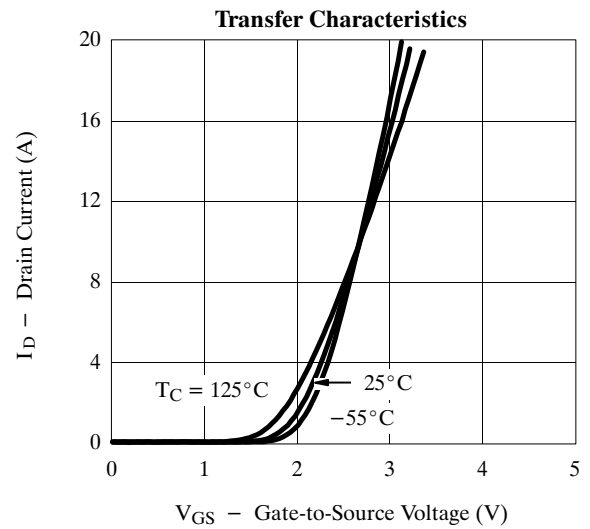
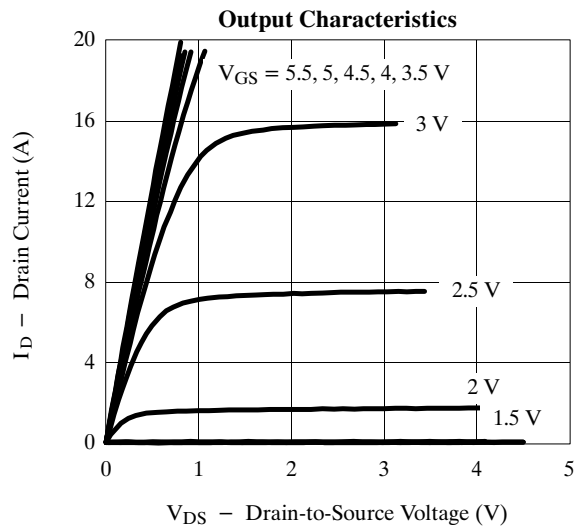
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.8			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 10\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 16\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 5\ \text{V}$	10			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 7.2\ \text{V}, I_D = 5.0\ \text{A}$	0.025	0.036	0.045	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 5.0\ \text{A}$		0.041	0.05	
		$V_{GS} = 3.0\ \text{V}, I_D = 3.9\ \text{A}$		0.050	0.07	
		$V_{GS} = 2.5\ \text{V}, I_D = 1\ \text{A}$		0.060	0.08	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 5.0\ \text{A}$		13		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 5.0\ \text{A}, V_{GS} = 0\ \text{V}$		0.9	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 6\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 5.0\ \text{A}$		10	20	nC
Gate-Source Charge	Q_{gs}			2.6		
Gate-Drain Charge	Q_{gd}			3.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\ \text{V}, R_L = 6\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		13	40	ns
Rise Time	t_r			9	30	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			9	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 5.0\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		100	150	

Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Si9925DY

Typical Characteristics (25°C Unless Otherwise Noted)

